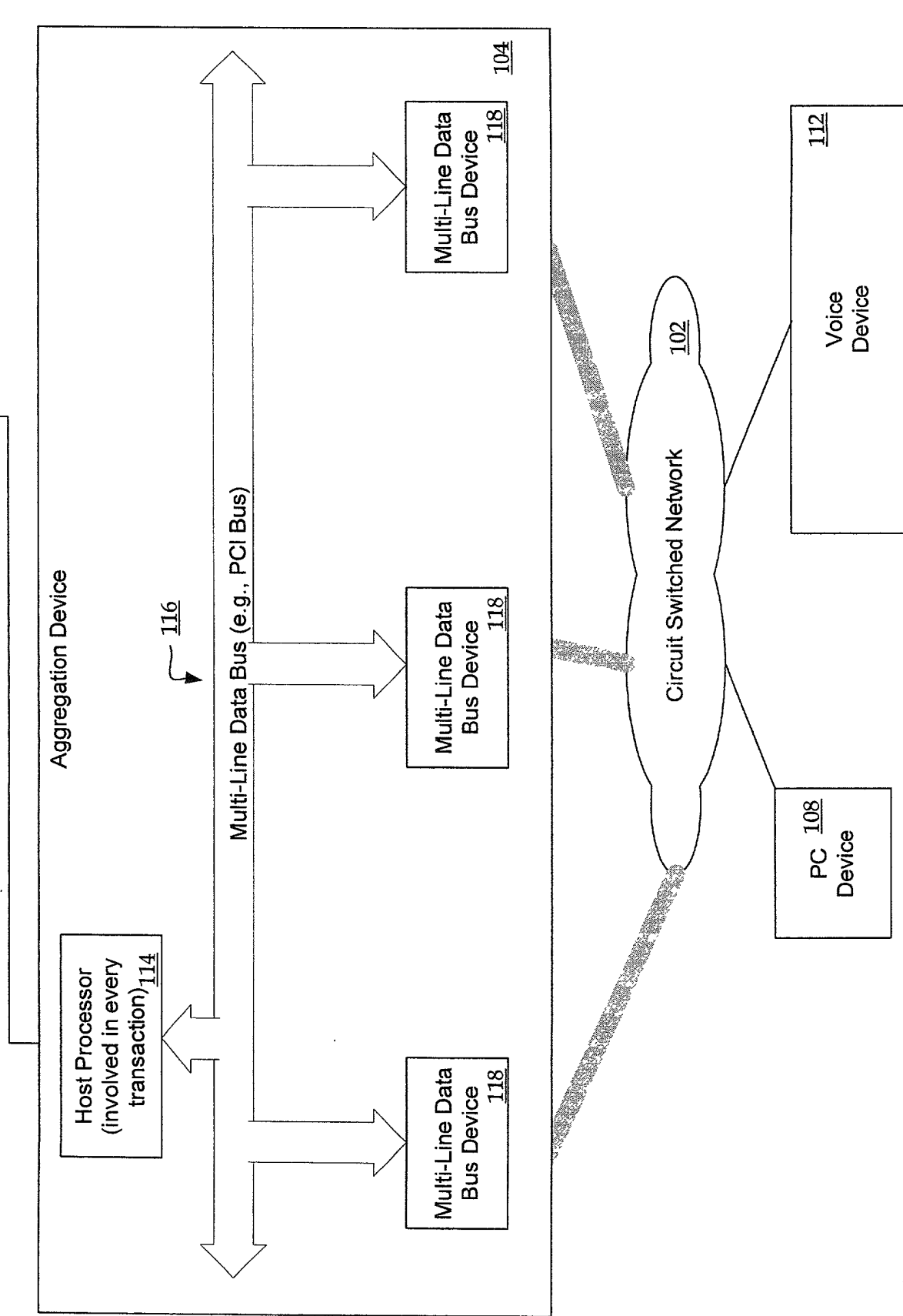


Fig. 1A
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Fig. 1B



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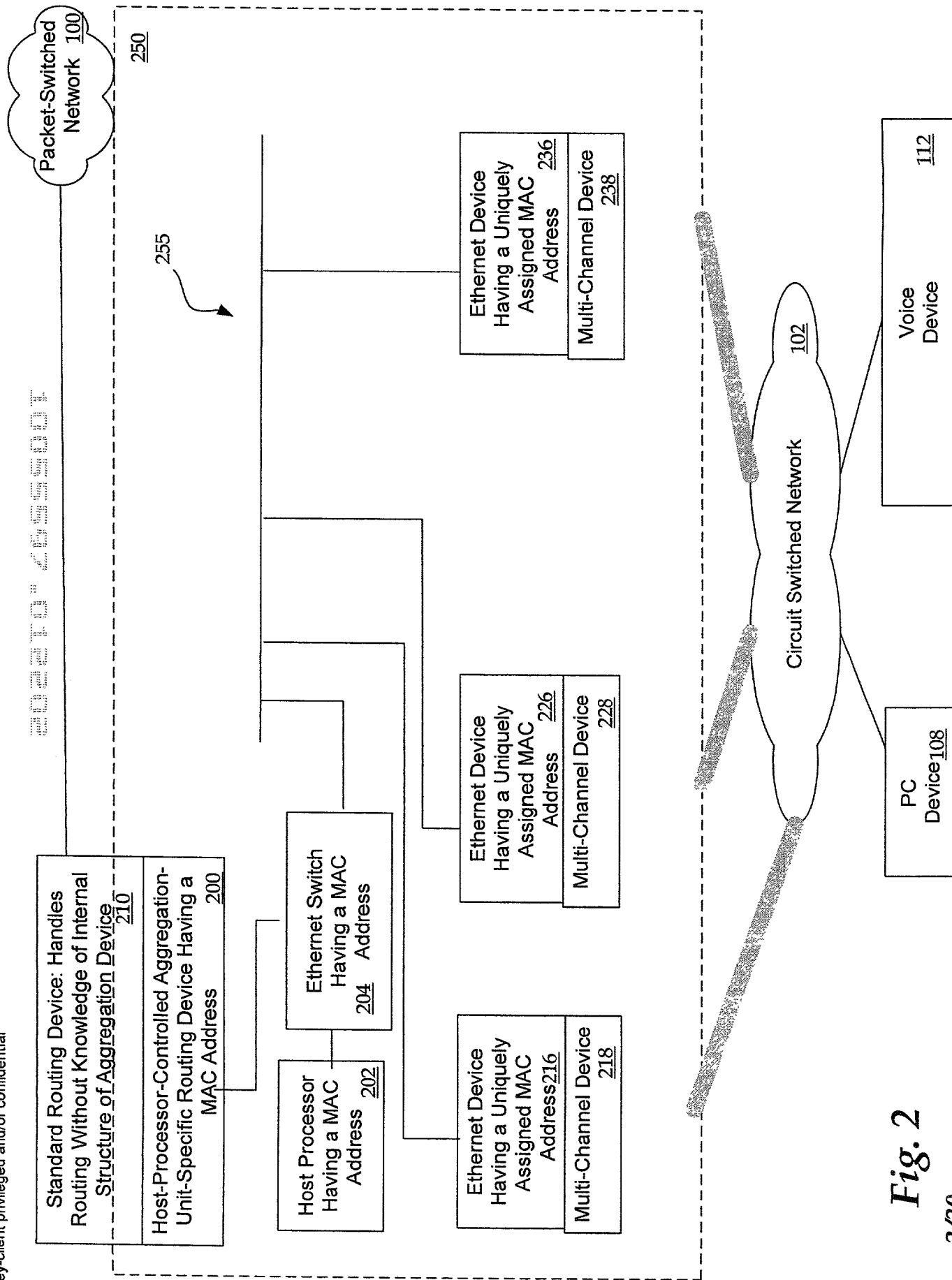
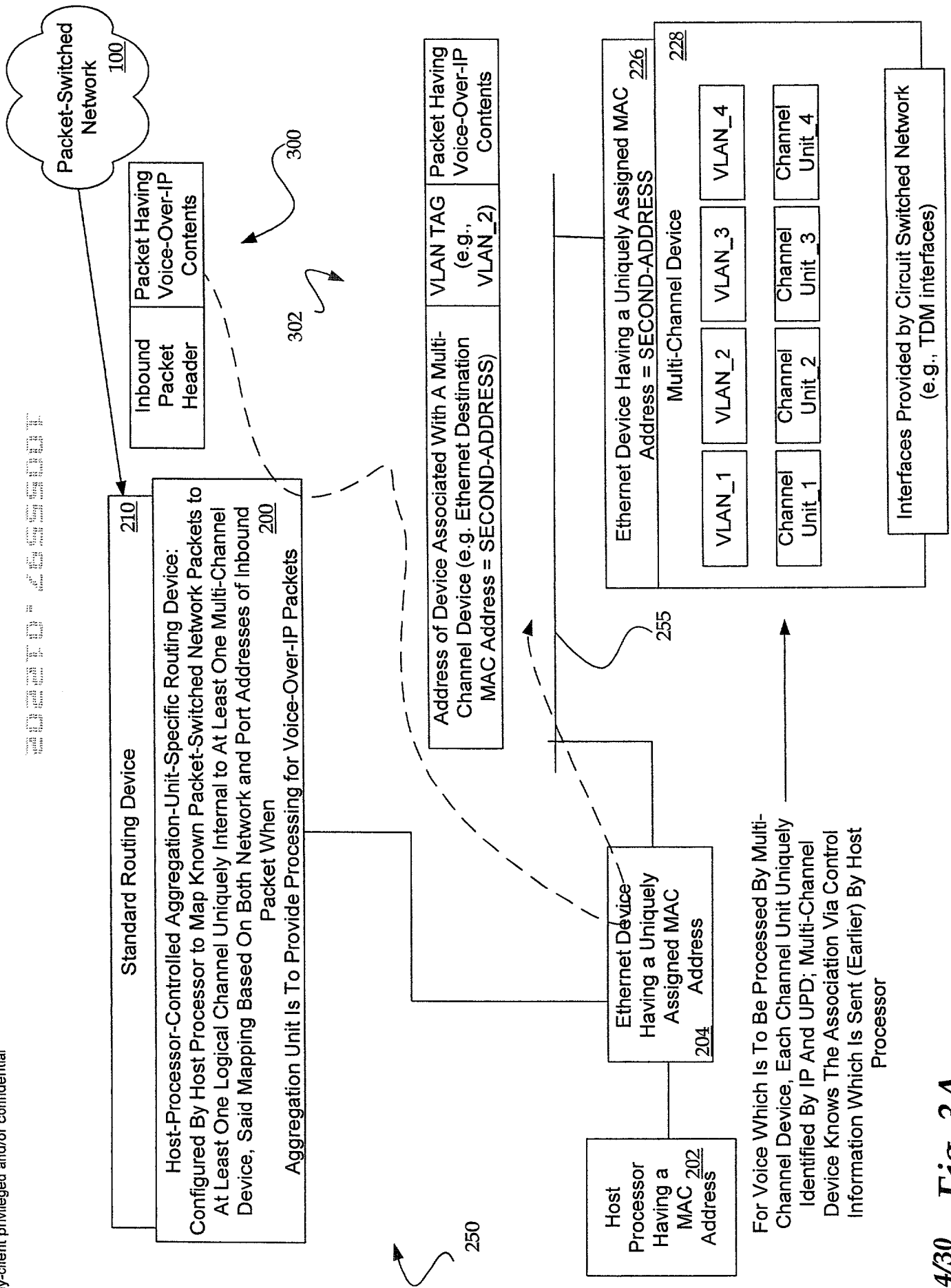
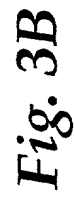


Fig. 2

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4/30 Fig. 3A



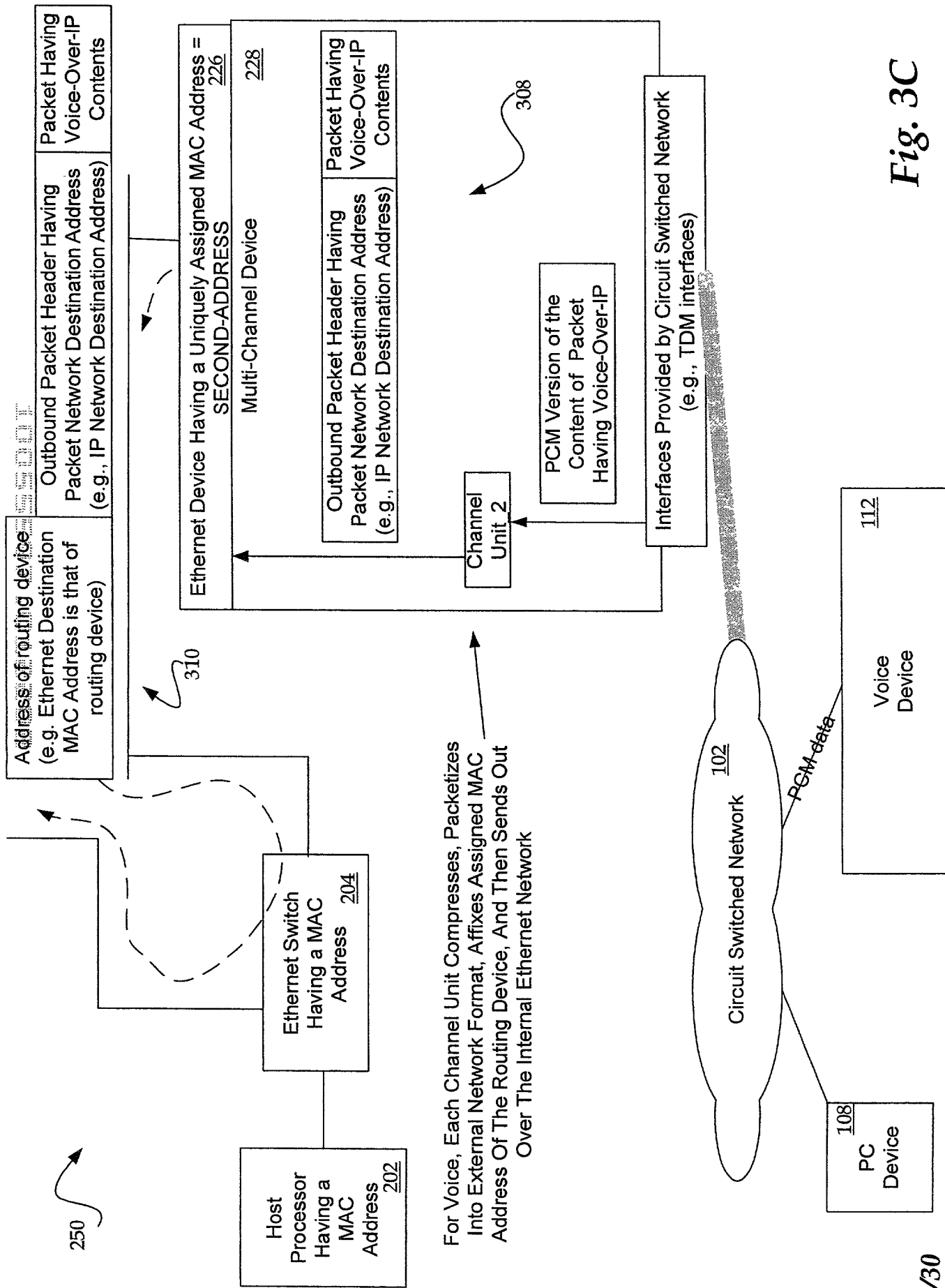
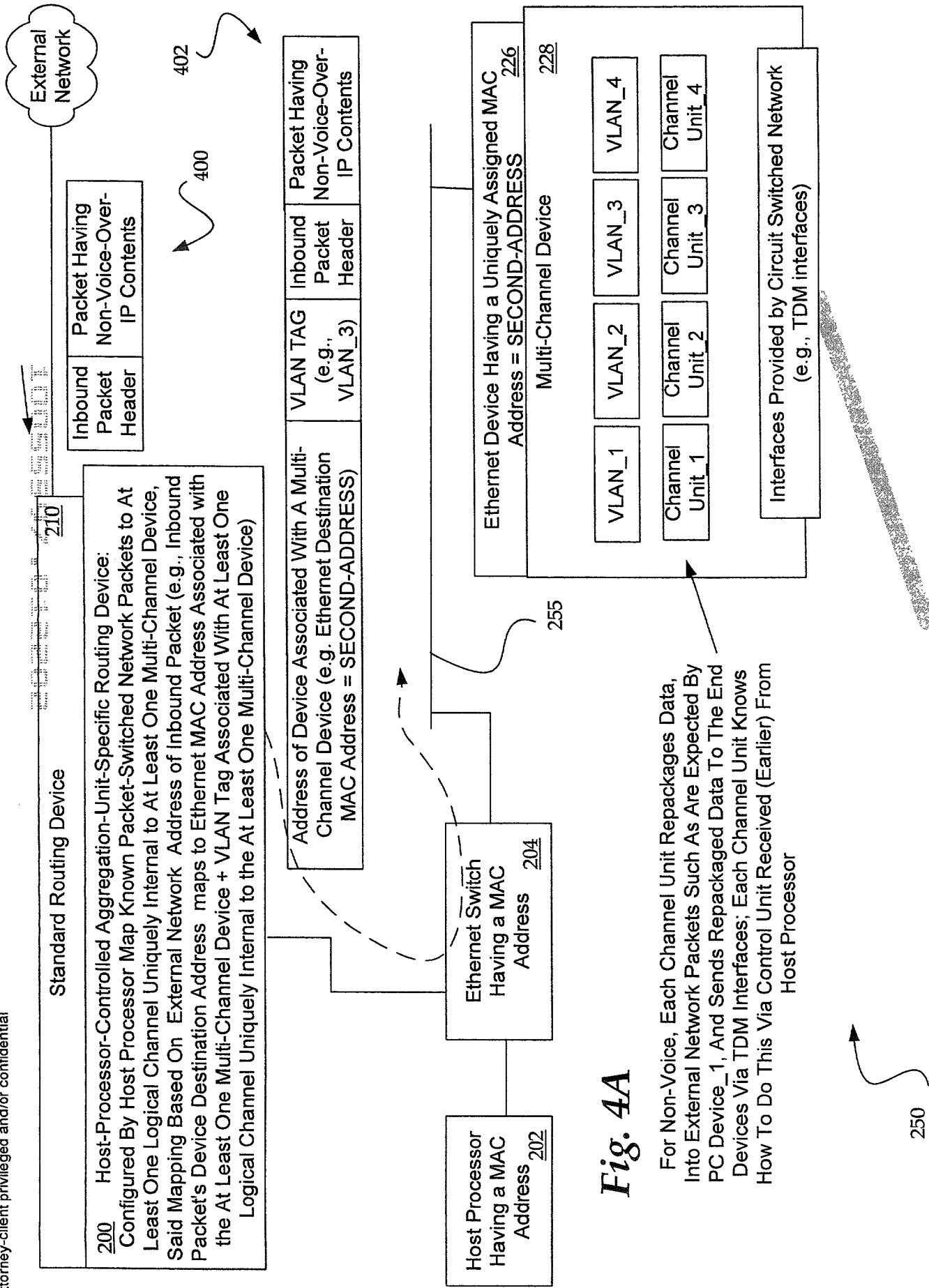
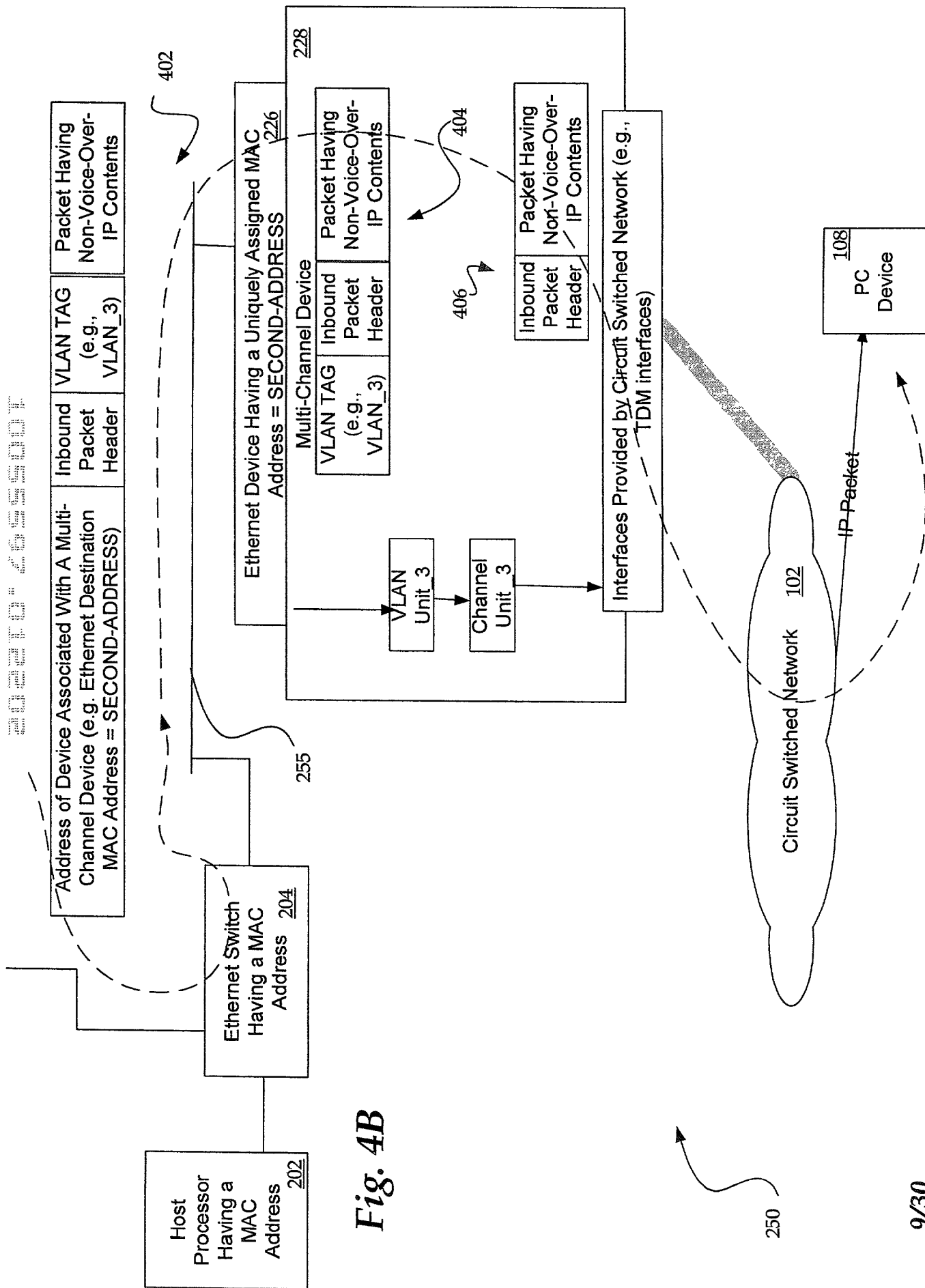


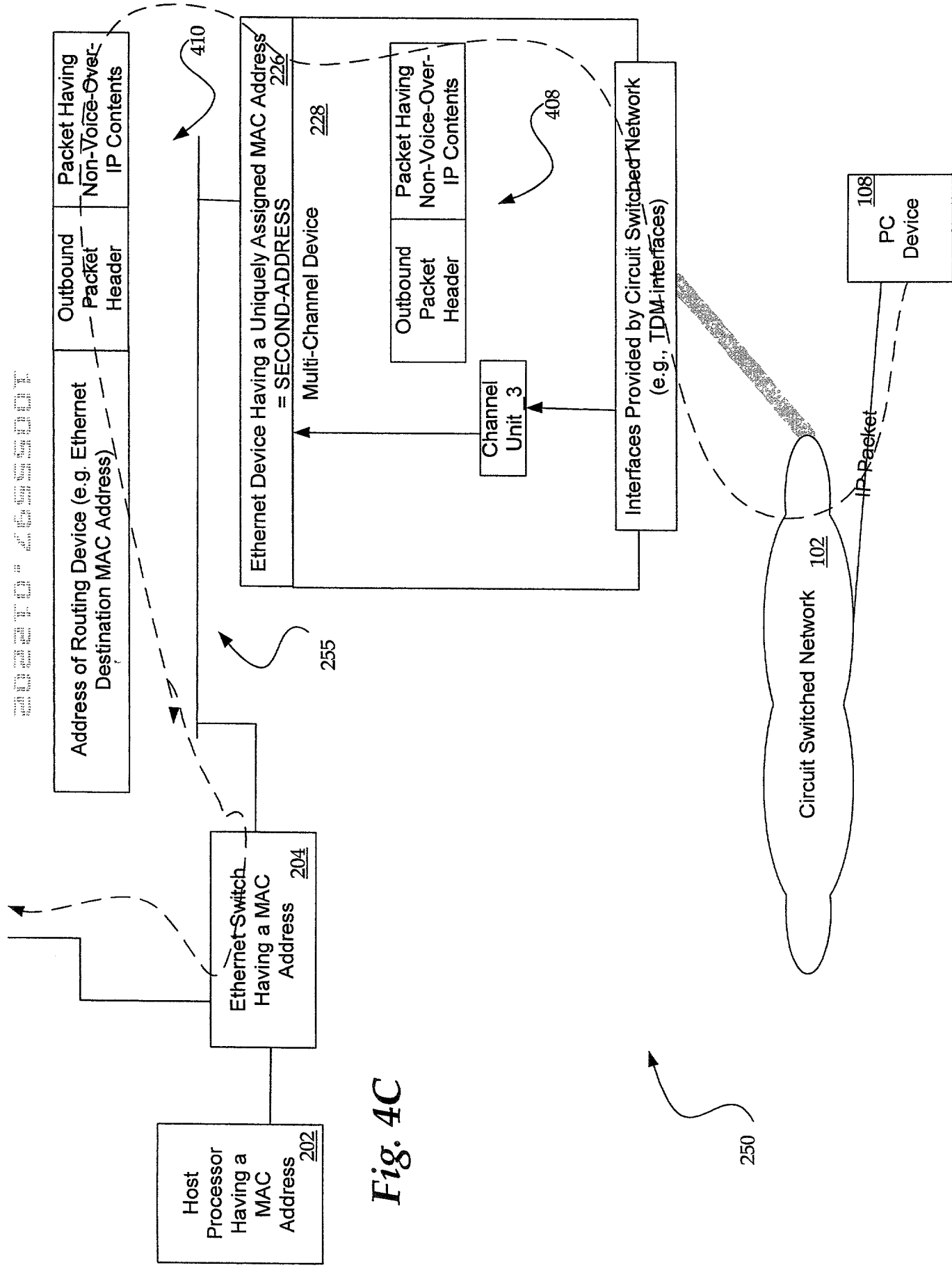
Fig. 3C



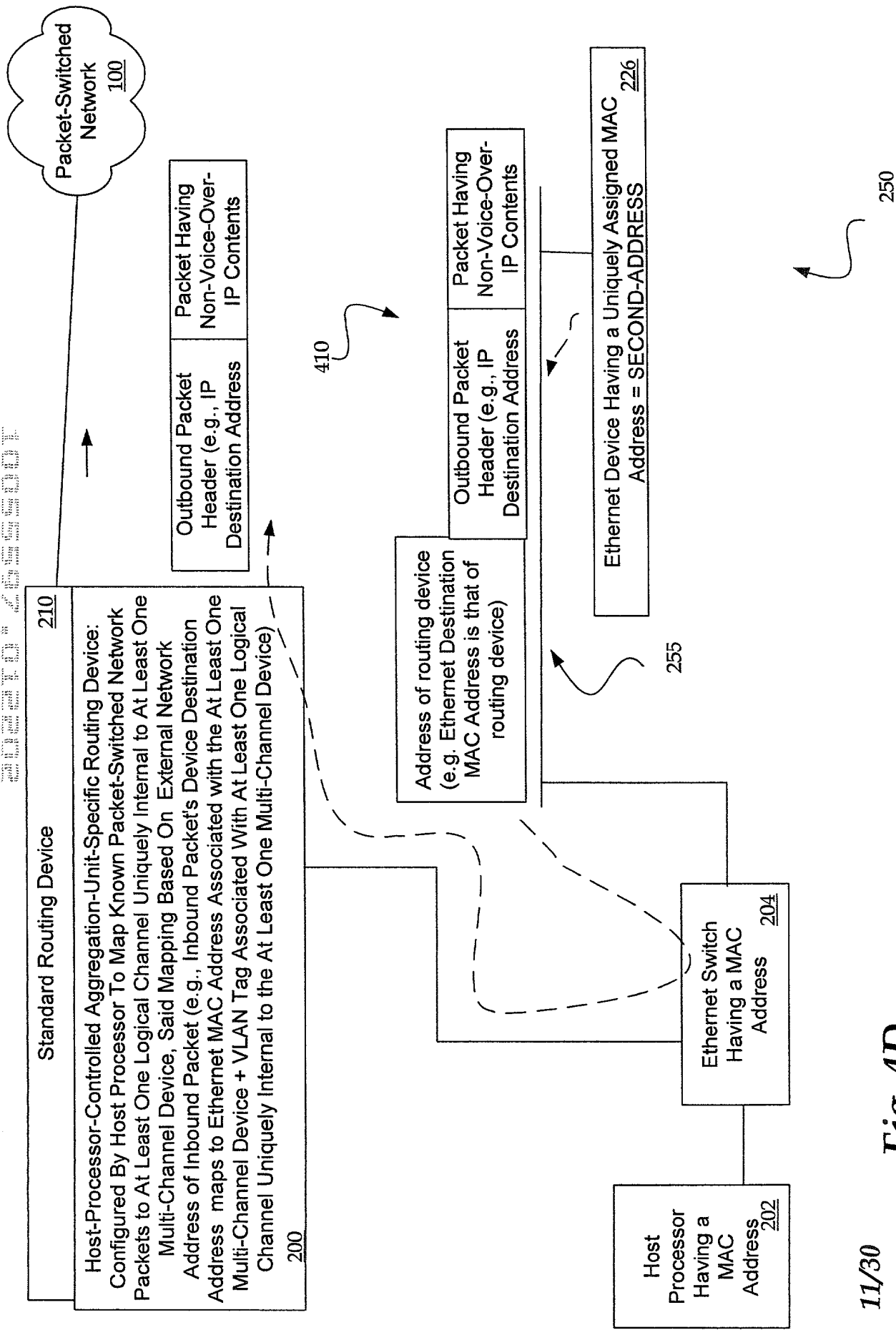
Fig. 3D

**Fig. 4A**



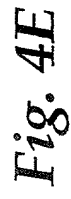


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Fig. 4D



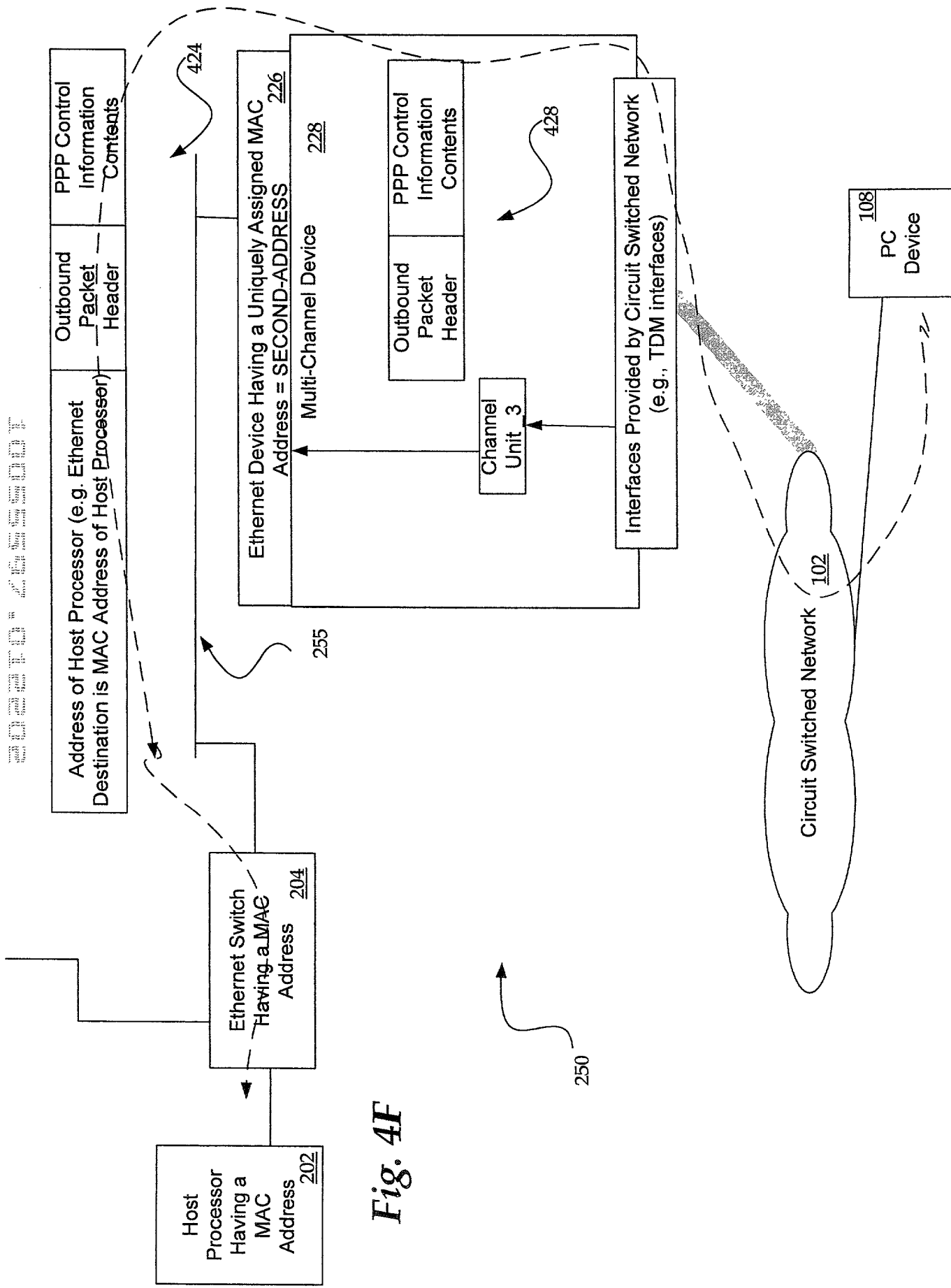


Fig. 4F

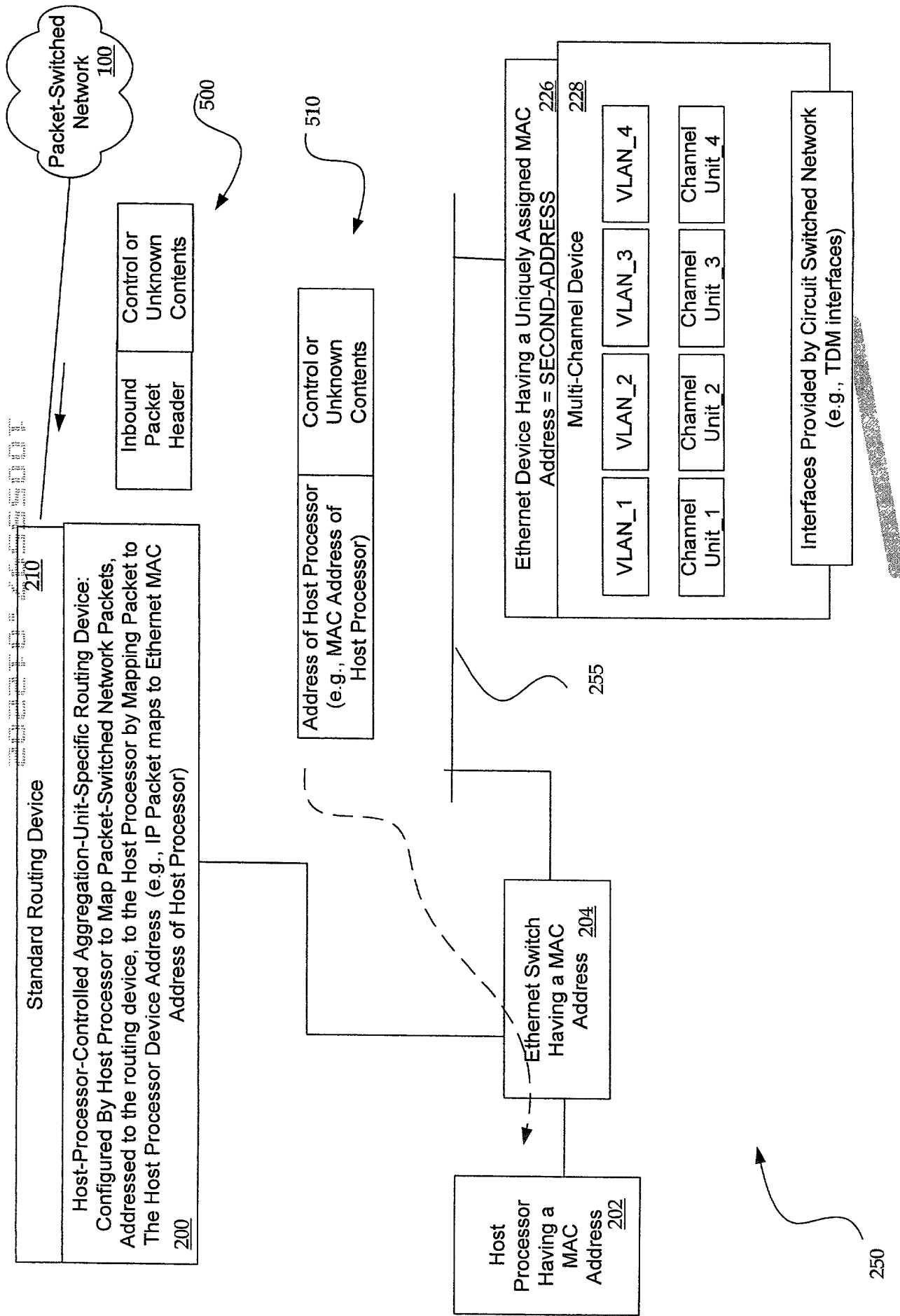


Fig. 5

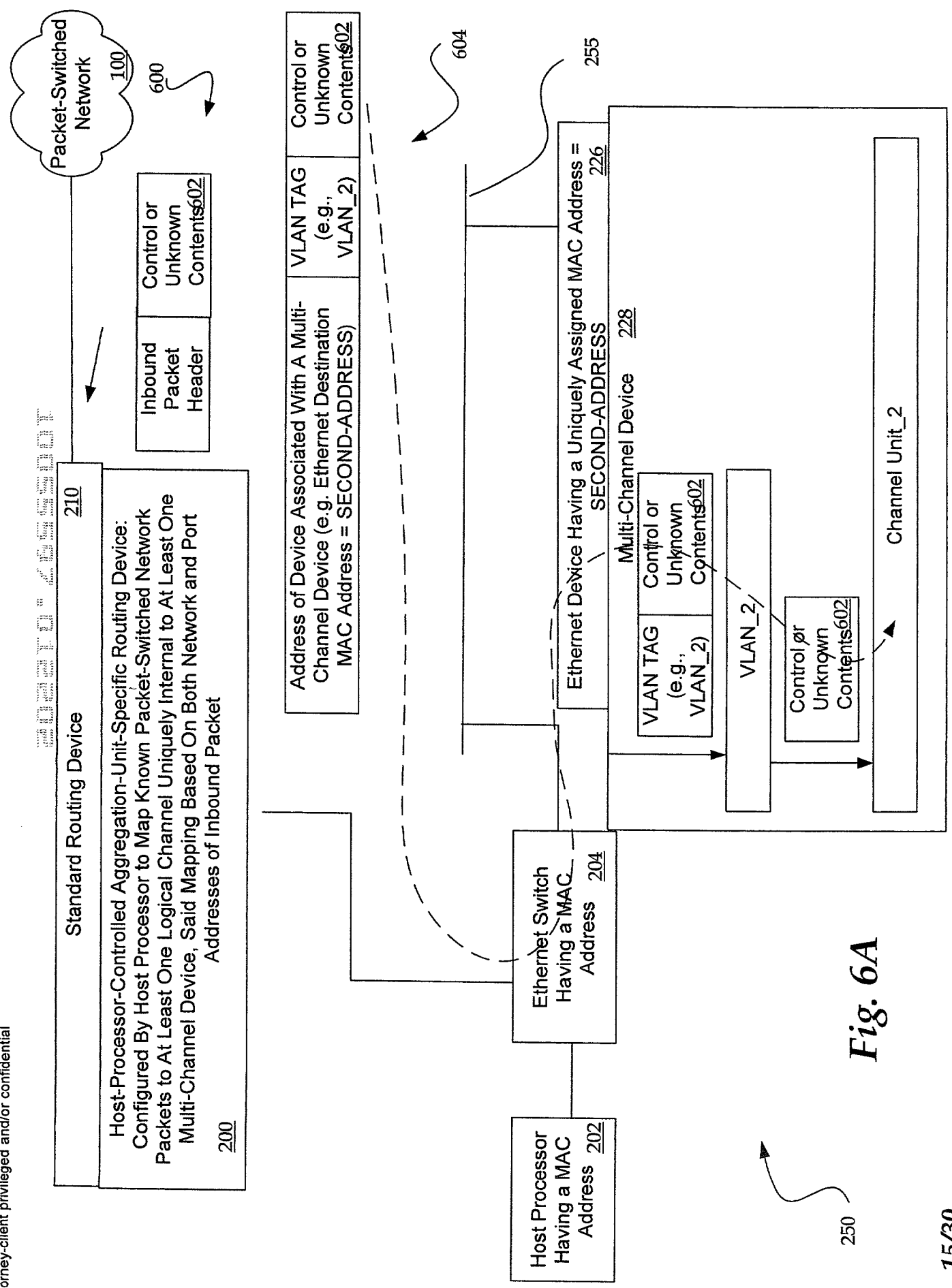


Fig. 6A

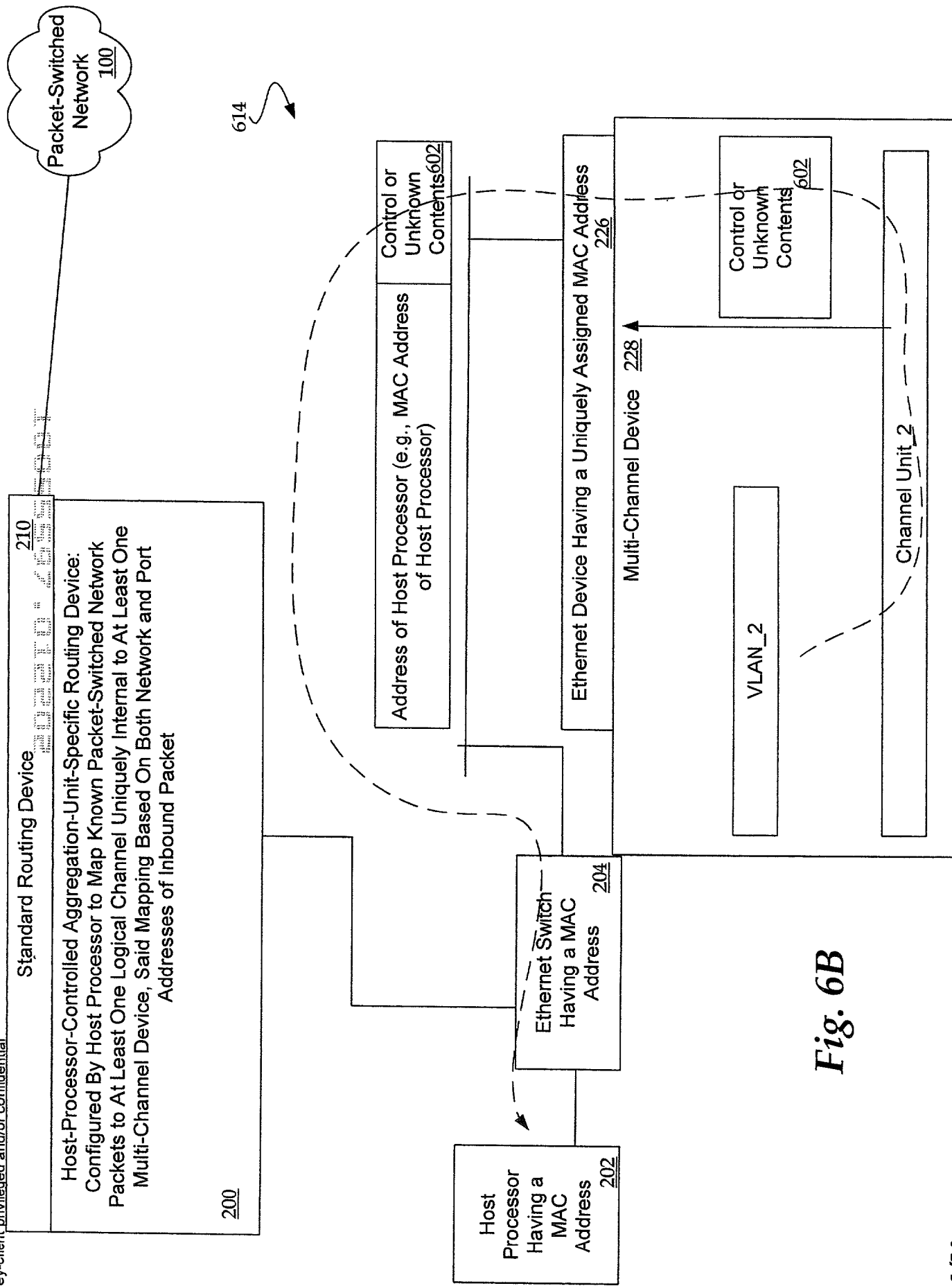


Fig. 6B

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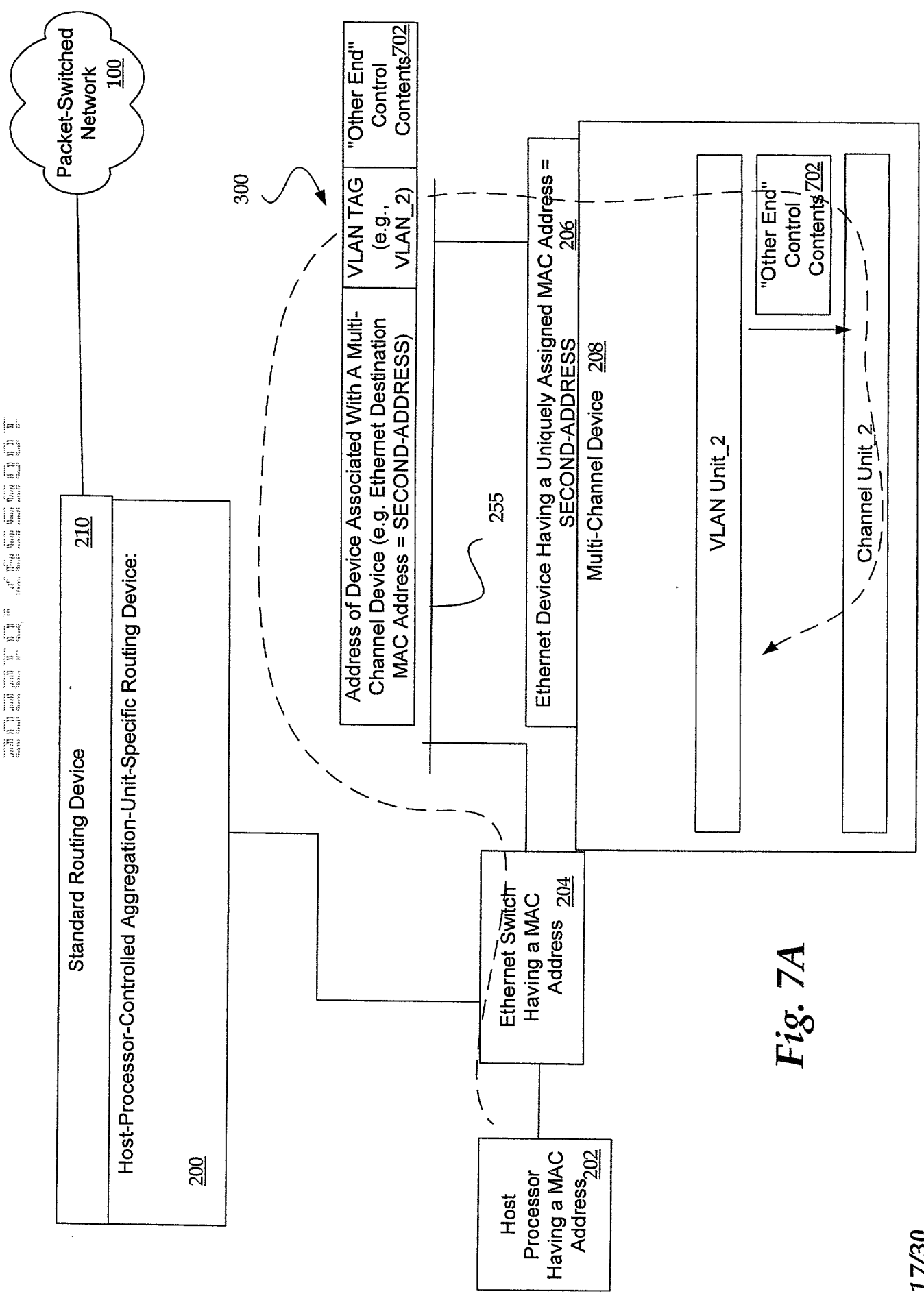


Fig. 7A

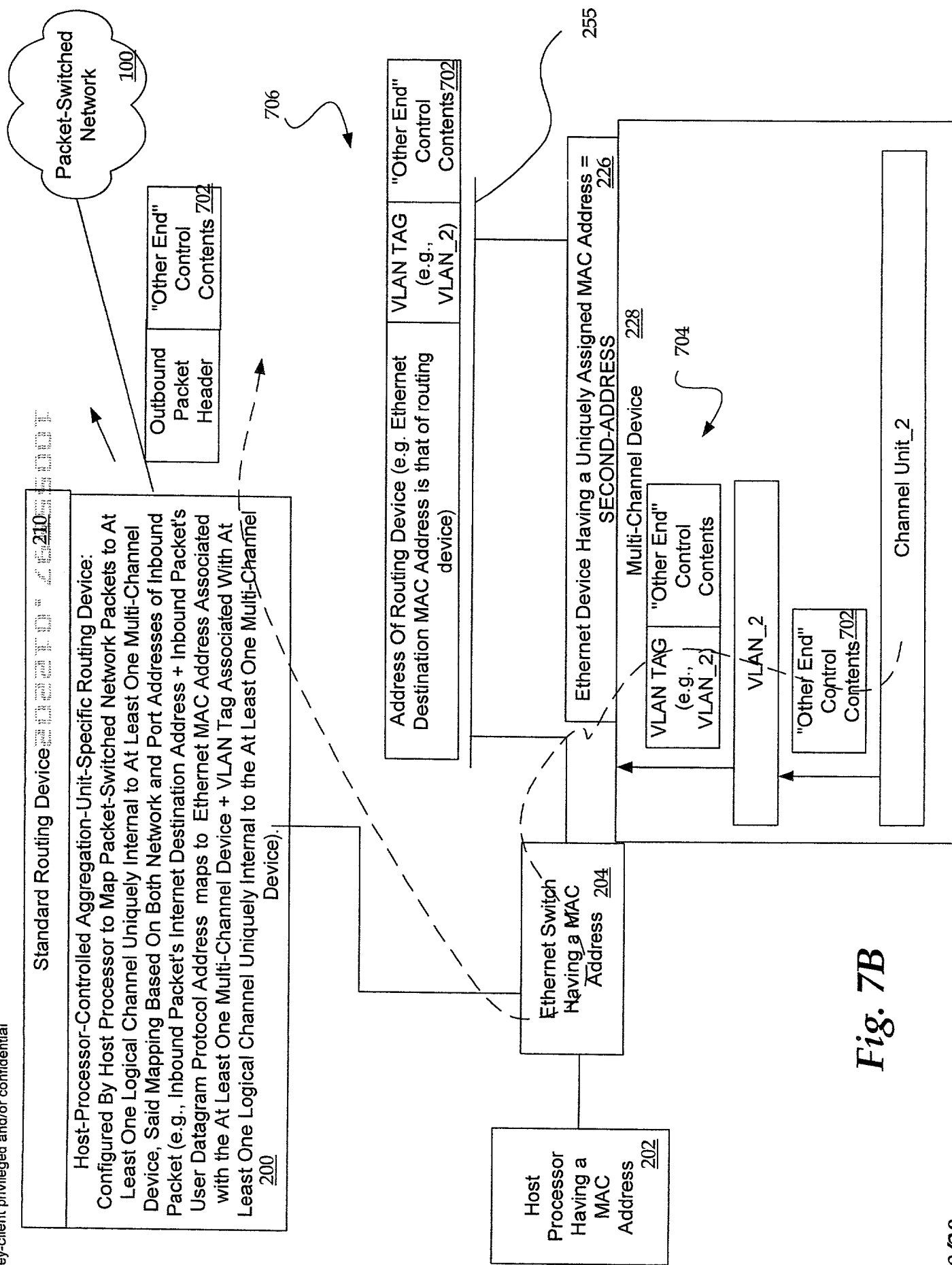


Fig. 7B

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Fig. 8A

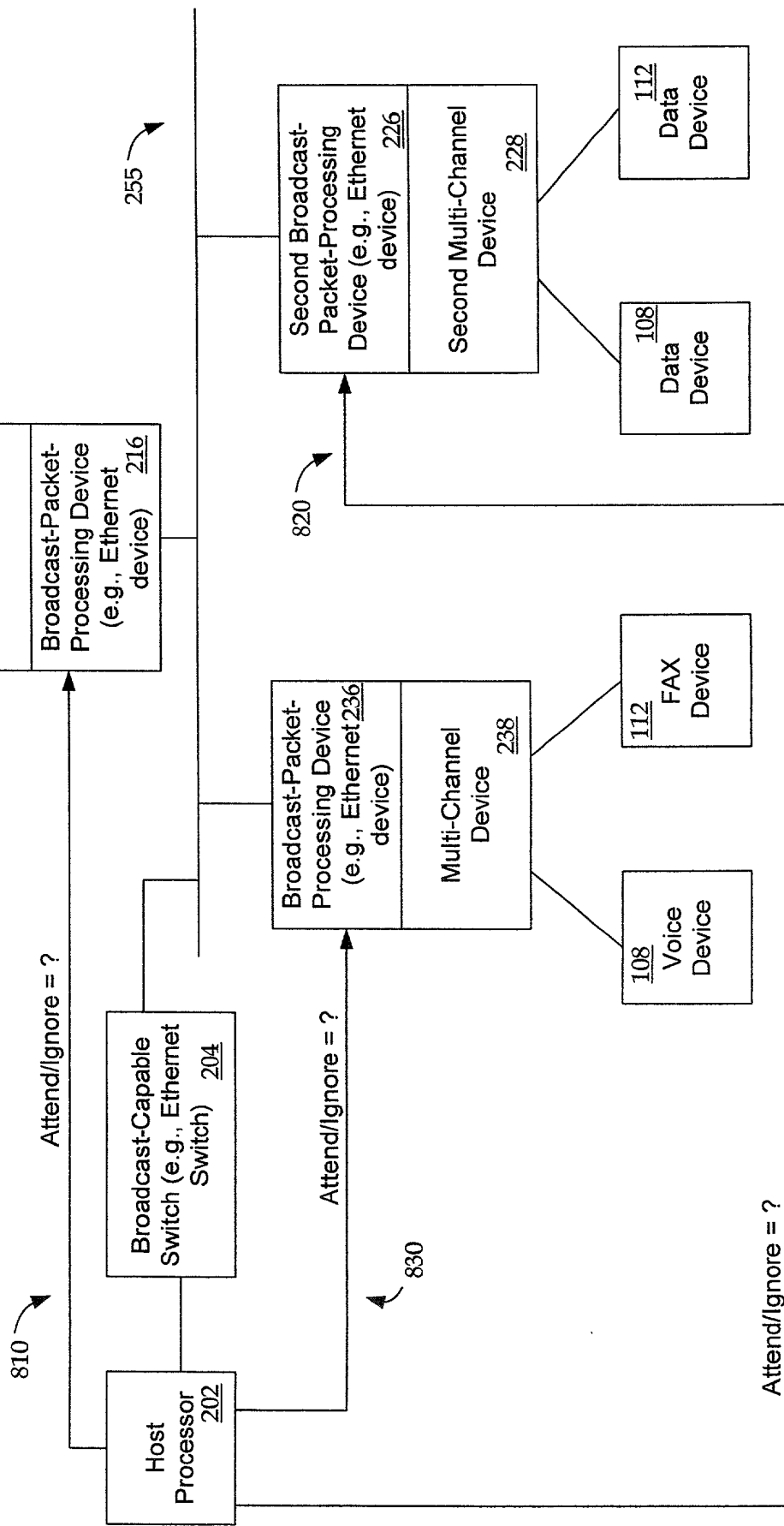
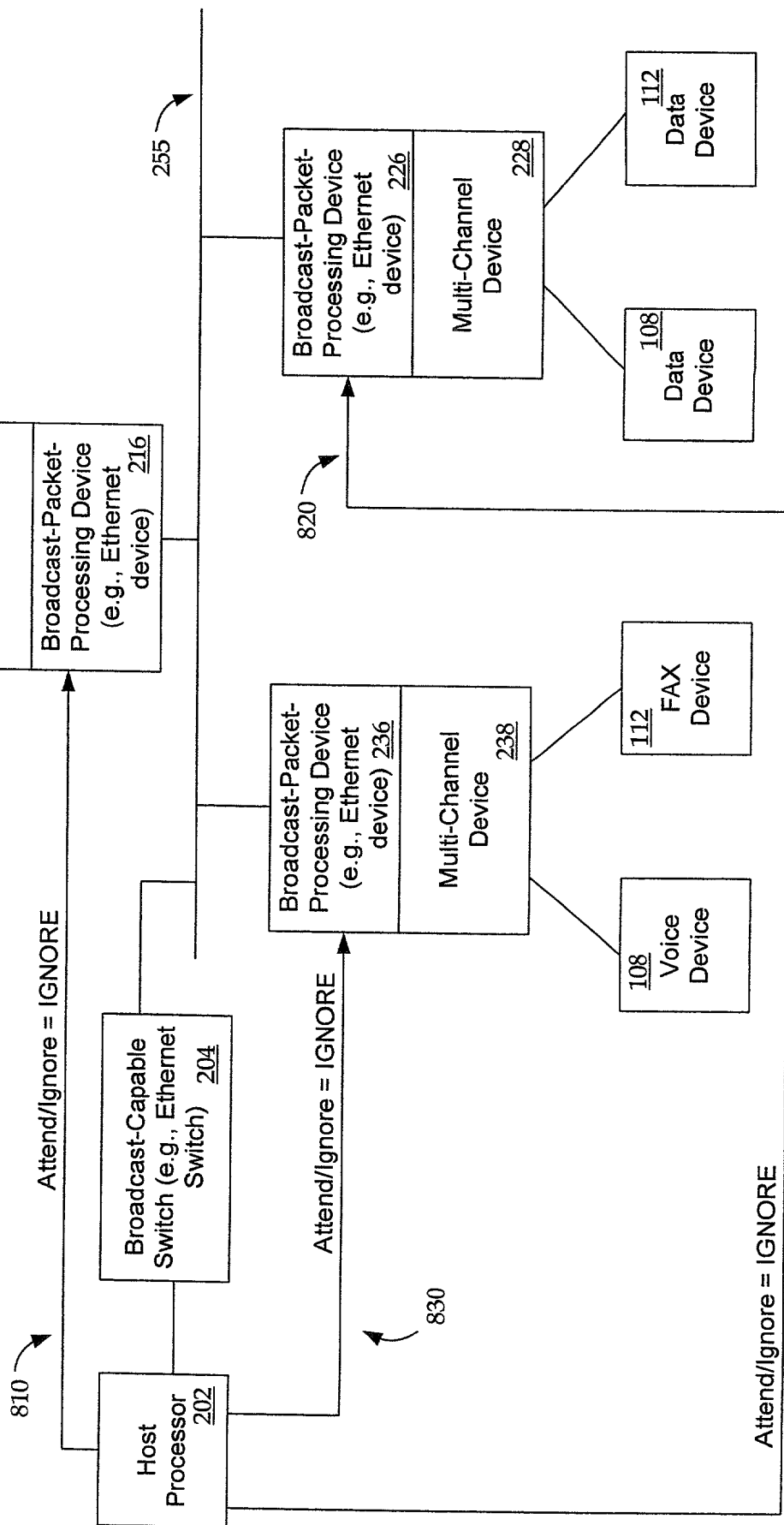
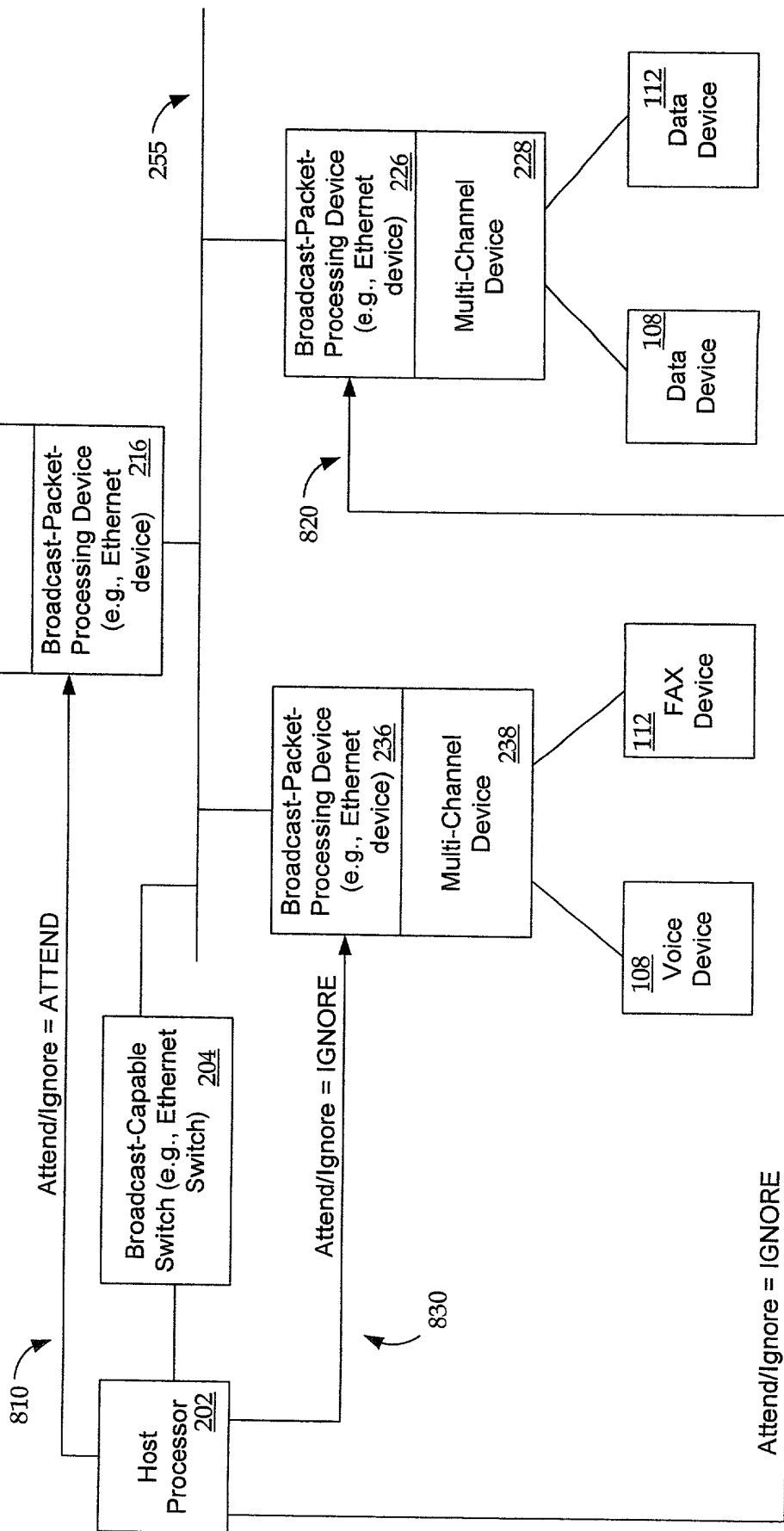


Fig. 8B



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Fig. 8C



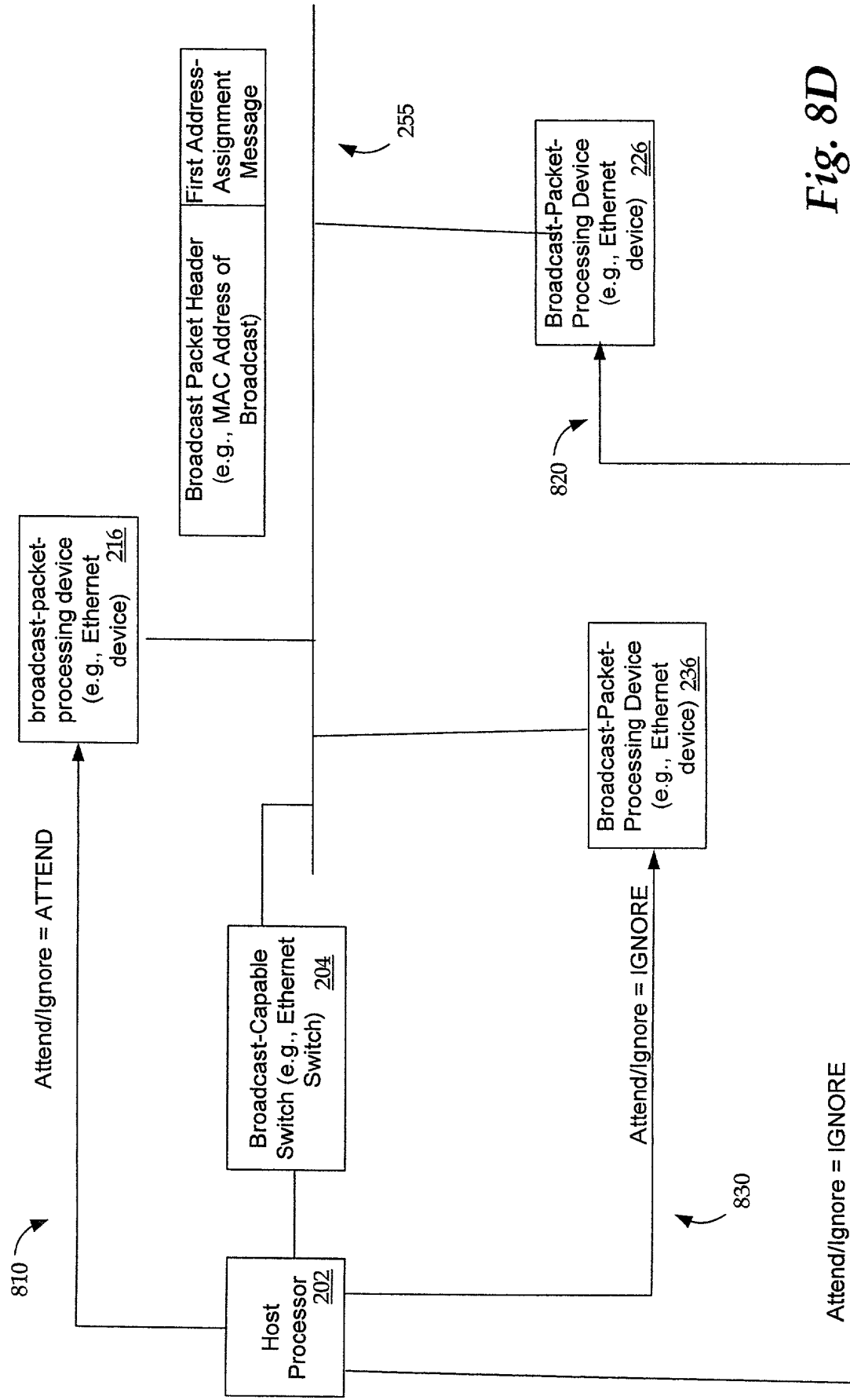


Fig. 8D

Fig. 8E

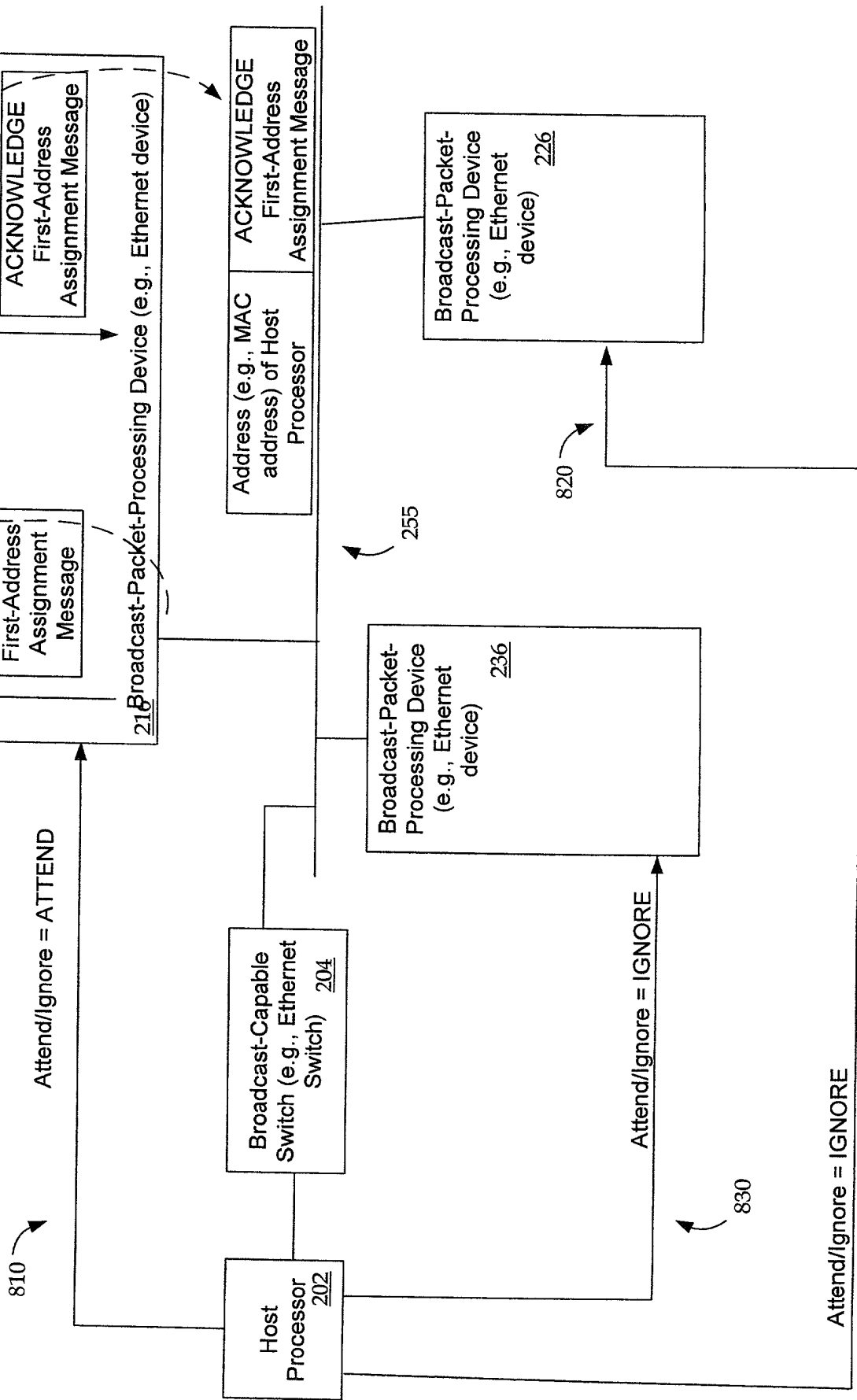


Fig. 8F

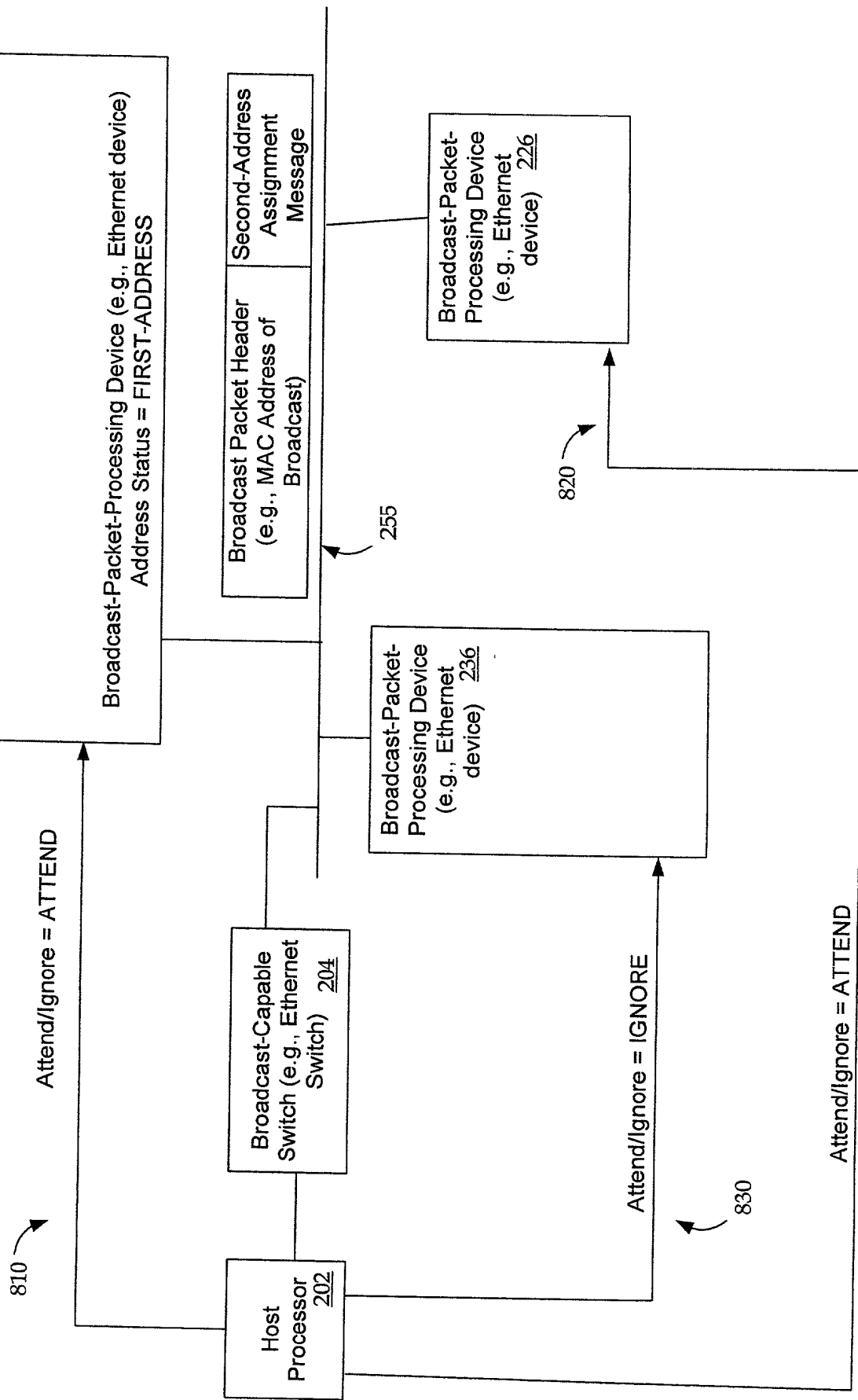


Fig. 8G

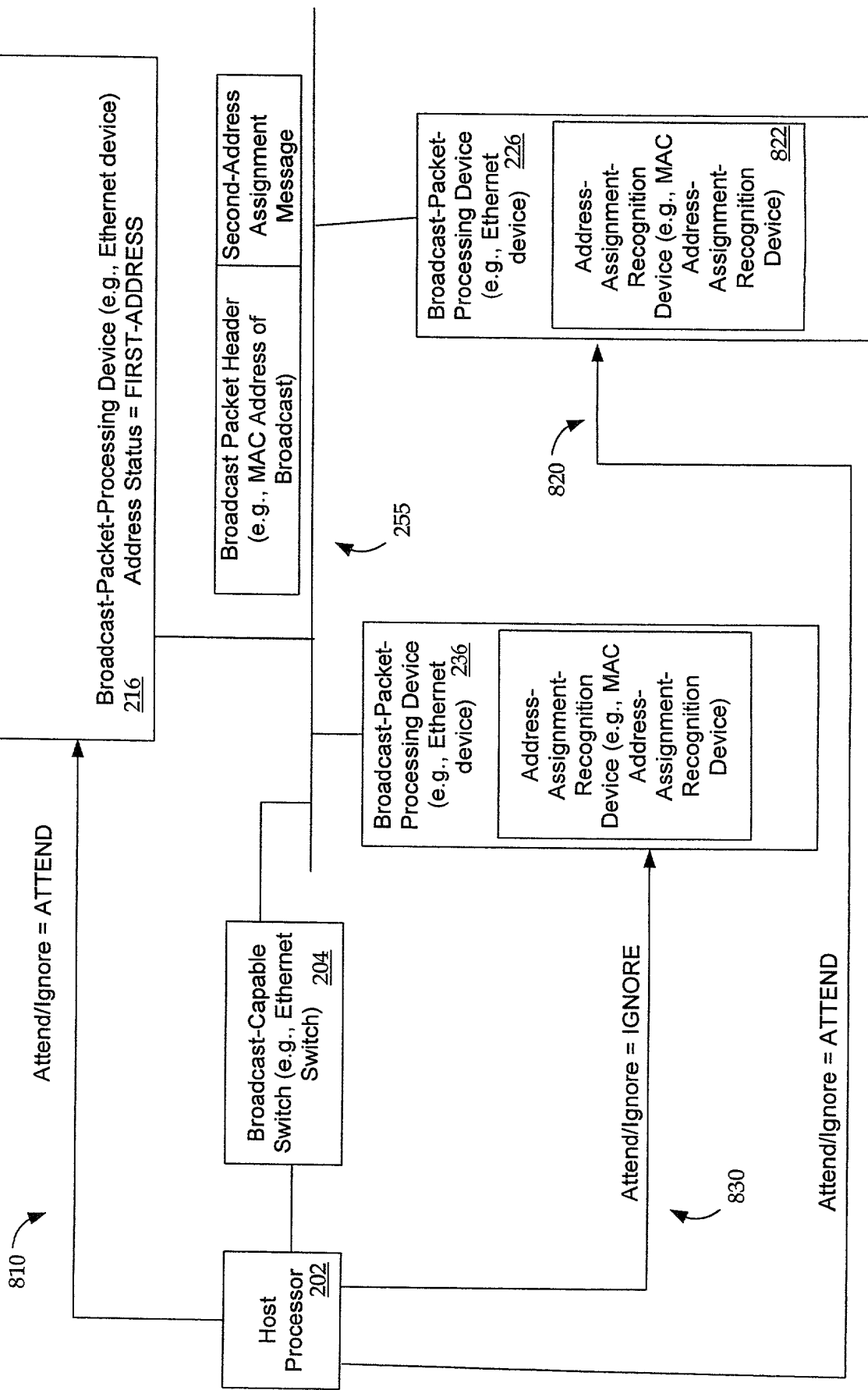


Fig. 8H

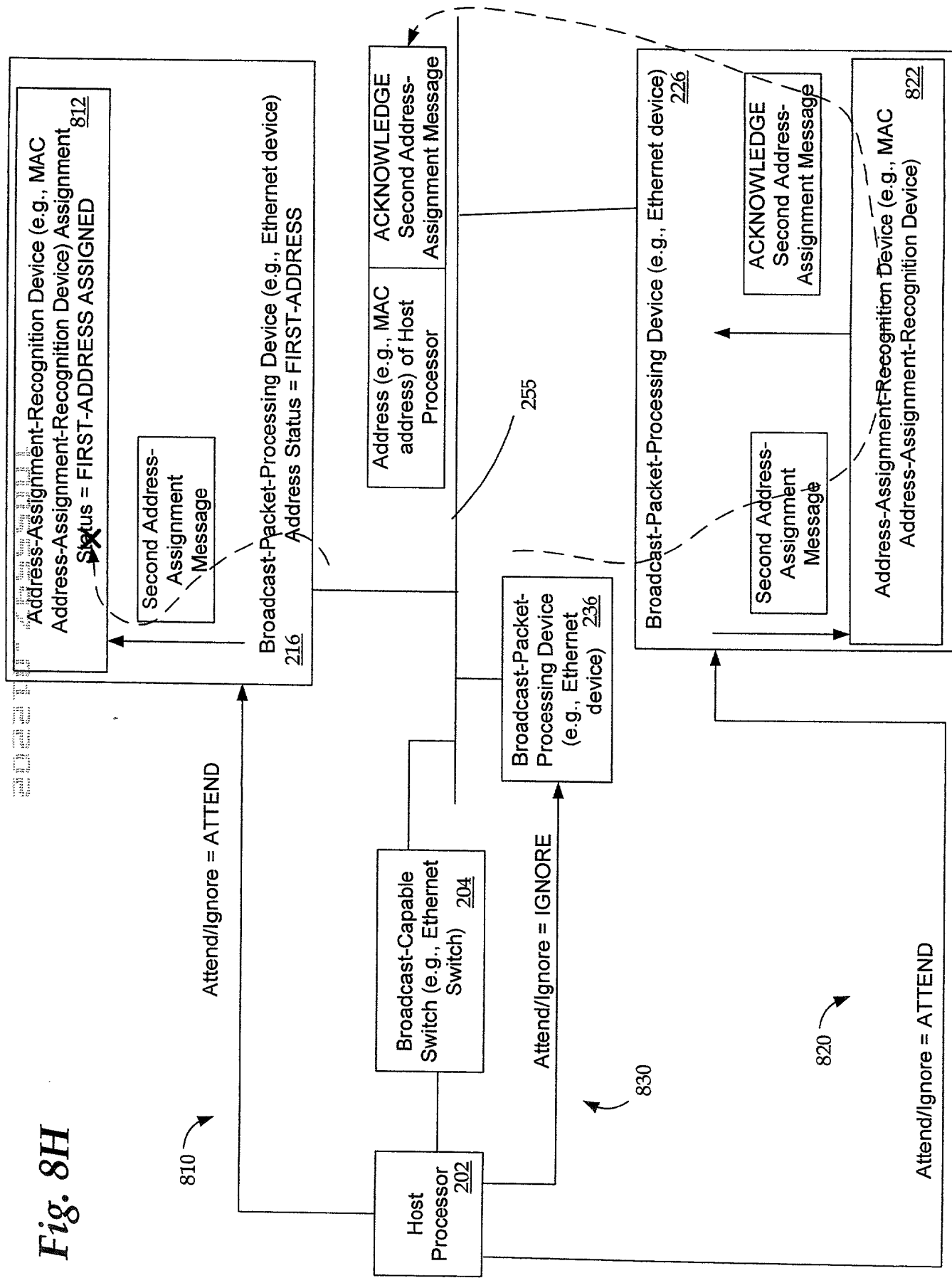
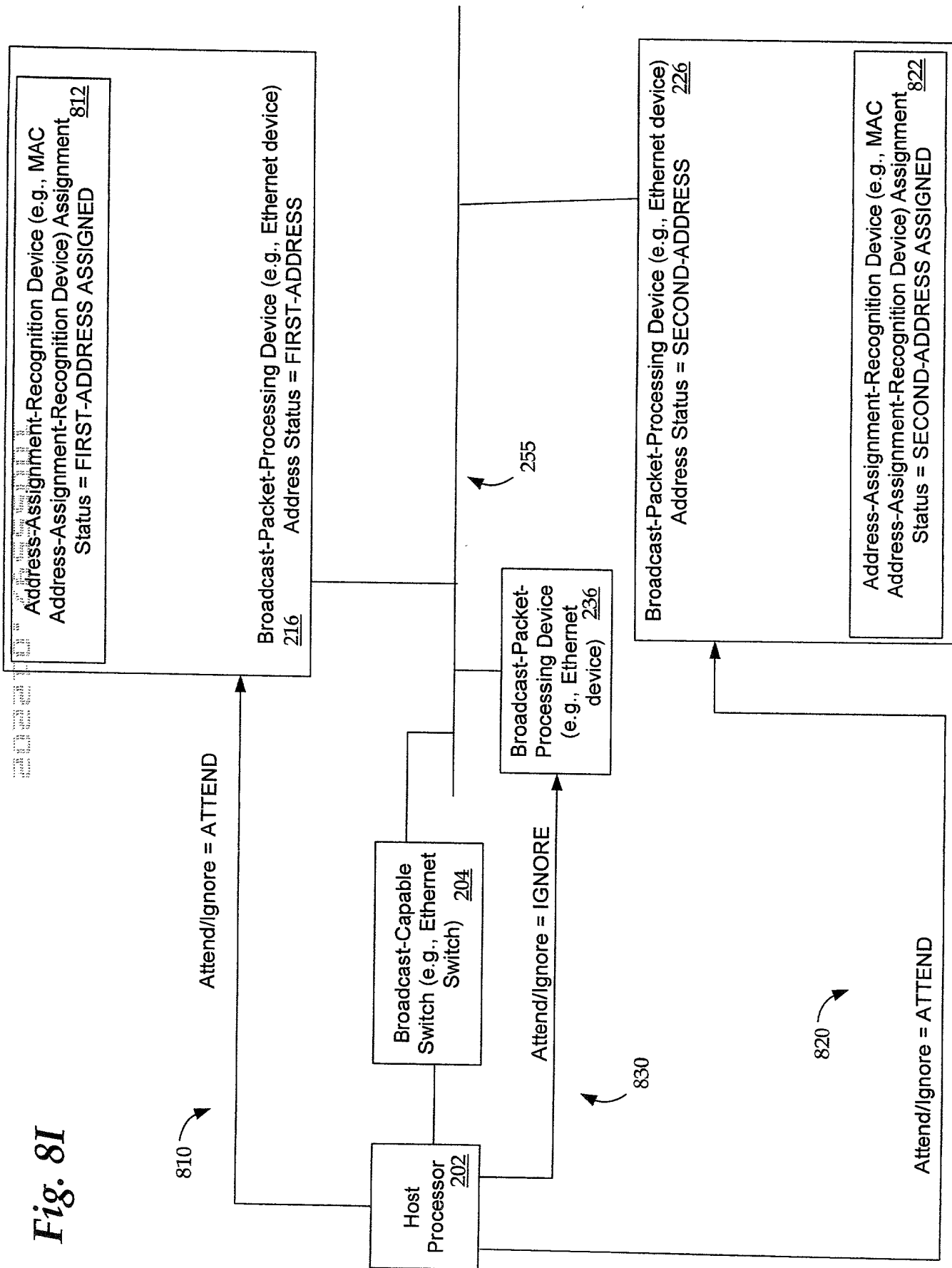


Fig. 8I



CONFIDENTIAL

Fig. 8J

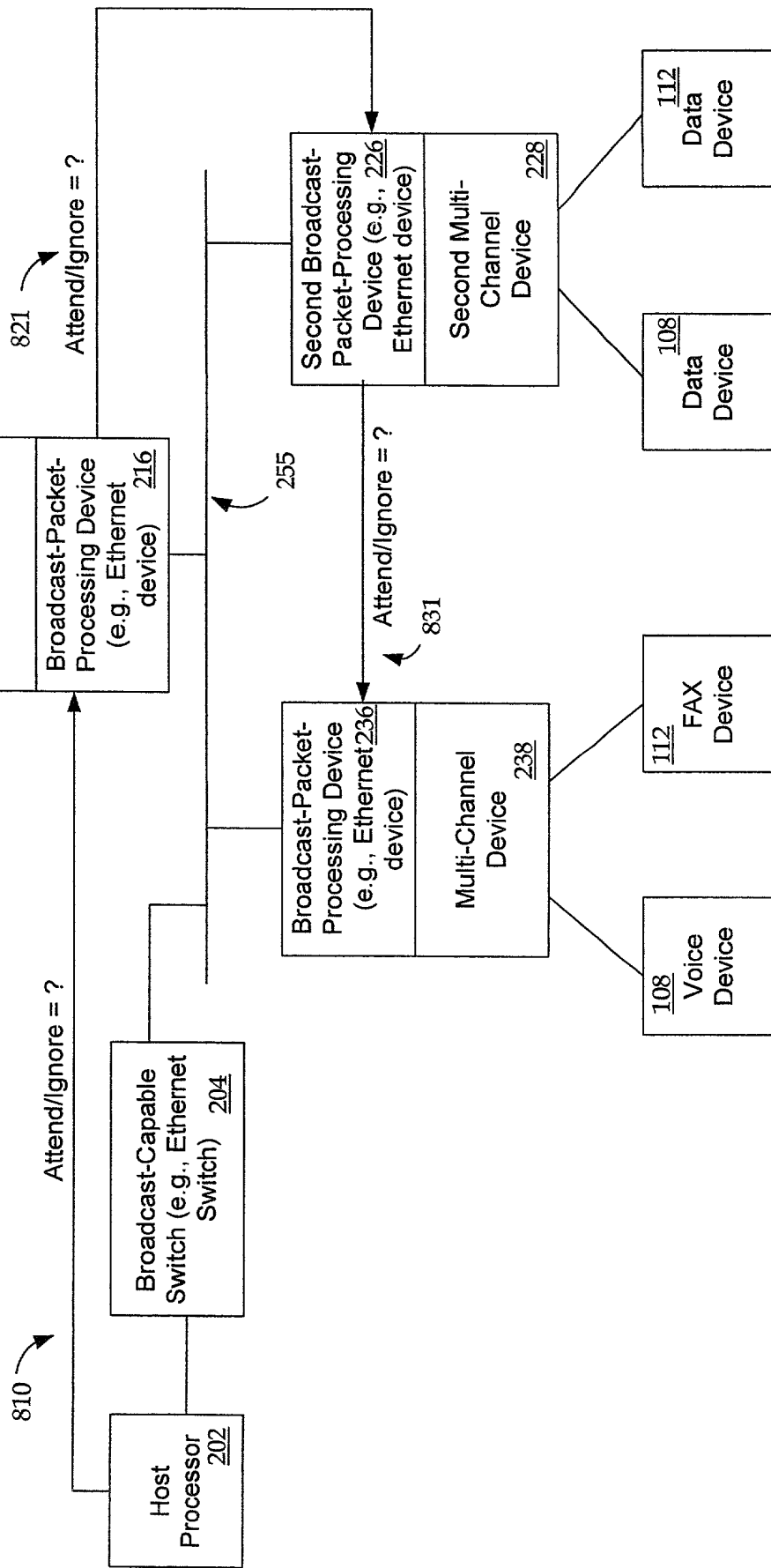


FIG. 9A

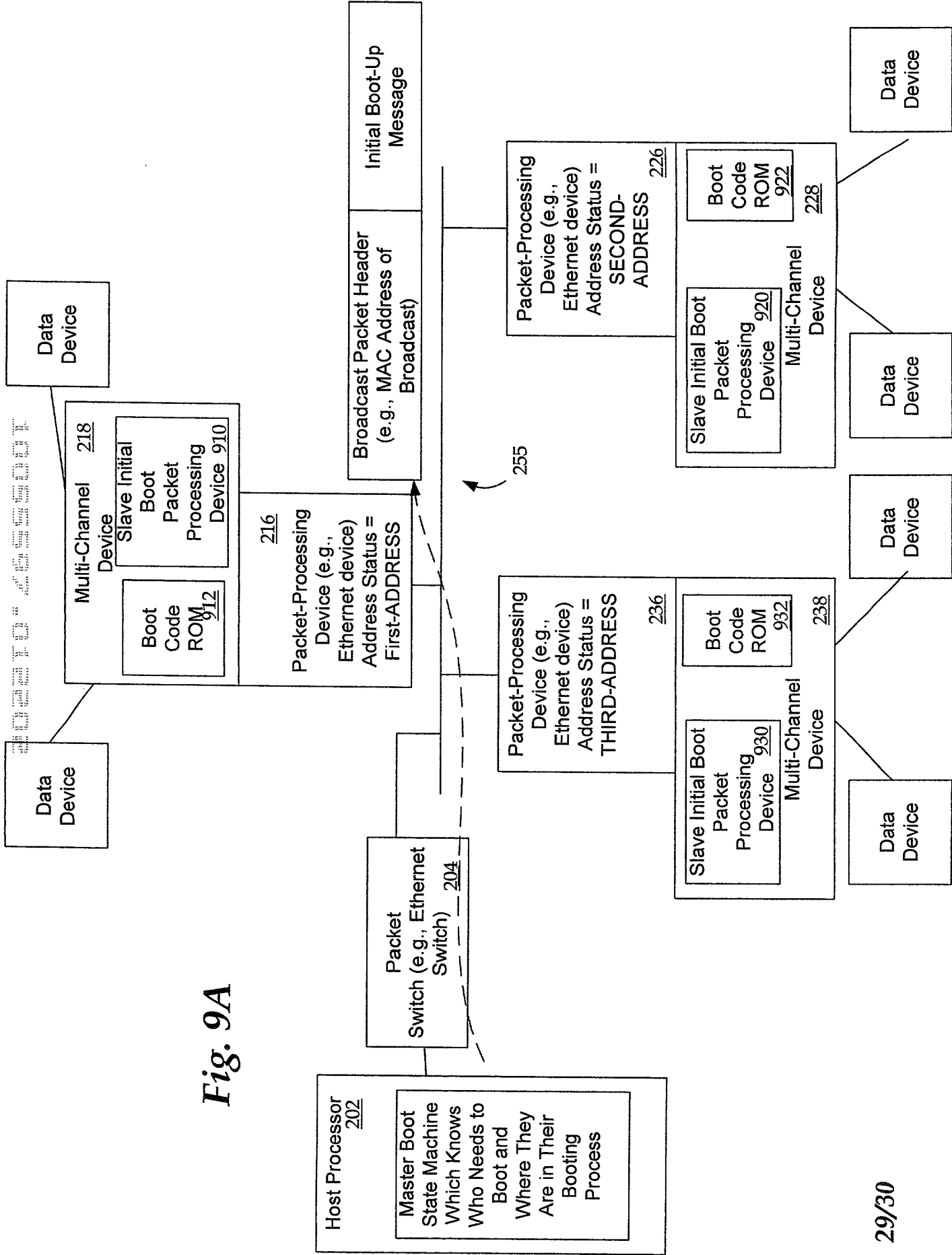


Fig. 9A

Figure 3 is a block diagram of a multi-channel booting system. The system includes a Host Processor 202, a Packet Switch (e.g., Ethernet Switch) 204, and three Packet-Processing Devices (e.g., Ethernet device) labeled 236, 226, and 228. Each Packet-Processing Device is connected to a Multi-Channel Device (238, 228, and 228 respectively). Each Multi-Channel Device contains a Slave Initial Boot Packet Processing Device (930, 920, and 920) and a Boot Code ROM (932, 922, and 922). Each Multi-Channel Device is connected to a Data Device. The Host Processor 202 is also connected to an Acknowledgment of Initial Boot-Up Message block.